FIG. **21** is a block diagram corresponding to claim **13**, which operates as follows.

1. A long code synchronized phase detector **64** includes in addition to the circuit as shown in FIG. **8** a comparator **65** for comparing B long code synchronized phases with the long code synchronized phase of a signal being demodulated now. The reference numeral **85** designates a dominant B correlation value selector (comparator), and **86** designates a memory for storing B long code synchronized phases.

2. As a result of comparison by the comparator **65**, if B detected long code synchronized phases coincide with the long code synchronized phase of the current demodulation signal, these phases are not input to a long code replica generator **66**.

With regard to claims **14** and **15**, FIG. **5** illustrates them, in which the timing controller **15** has a plurality of mask symbols generated at various timings.

FIG. **22** is a block diagram corresponding to claim **16**, which operates as follows.

1. A long code synchronized phase detector **67** has a matched filter **69** and a memory **70** inserted after a memory **82** for storing correlation values and timings. The matched filter **69** includes patterns of mask symbols and the memory **70** stores the correlation values and timings passing through the matched filter.

2. Correlations between the spread modulation signal and a short code are detected for one or more long code periods, and the resultant correlation values and their timings are stored in a memory **82**.

3. After storing, a correlation value sequence is input to the matched filter **69** which is matched to the insertion interval of the mask symbols to obtain the correlation sums at the respective timings (see, FIG. **15**).

4. The resultant correlation sums and timings are stored in the memory **70** for storing them.

5. After completing the detection at all the timings, a maximum correlation value selector **83** selects the maximum correlation sum and its timing which is made the synchronized timing.

6. The operation after this is the same as that of claim **4** or others.

FIGS. **25**A and **25**B show the synchronization detector of the spreading code synchronization method associated with claim **20** of the present invention. Although the operation of a long code timing detector **90** is similar to that of the long code synchronized phase detector **35** of FIG. **17**, it employs a shared short code replica generator **91** instead of the short code replica generator **81** because it uses group codes in addition to shared short codes, as the short codes. A memory **84** in the long code timing detector **90** outputs the received timings of a signal spread by a known group code in the received signal, in response to the received timings of the long code which gives the maximum correlation. Group code replica generators **93** are provided by the number of group codes (three in FIGS. **25**A and **25**B) in a long code group timing detector **92**, and generate group code replicas to be multiplied by a received signal at received timings of the corresponding group codes fed from the memory **84**. The resultant product signals are integrated over one symbol period by integrating/dumping circuits **94**, and square-law detected by square-law detectors **95**. The resultant square-law detected values of the correlation integrals associated with the group codes are stored in a memory **96**. The foregoing operation is performed on a plurality of signals spread by received group codes, and the results are stored in the memory **96**. After completing the correlation detection, a detector **97** obtains, in accordance with the transmission patterns of group code candidates, correlation value sums of the square-law detected values of the correlation integrals whose number equals (the number of the group codes output from the memory **96**)×(the number of times of correlation detection). The method for obtaining them was described before in connection with FIG. **24**. A selector **98** compares the correlation value sums whose number equals the number of transmission patterns of the group code candidates obtained, and selects the pattern giving the maximum correlation value. Then, a long code group detector **99** detects a long code group including the long code for spreading the received signal from the pattern output from the selector **98**. Then, the spreading code synchronization detection proceeds to the long code identification. The operation of a long code identification circuit **100** is the same as the foregoing spreading code synchronization method in accordance with the present invention, in which the long code is detected as follows: First, a multiplier multiplies the received signal by the code obtained by multiplying the long code fed from a long code replica generator **101** by a short code fed from a shared short code replica generator **91**; second, an integrating/dumping circuit **102** integrates the resultant product and a square-law detector **103** square-law detects the integral output; and finally a threshold value decision circuit **104** makes a threshold decision. The operation of the threshold value decision circuit **104** is the same as that of the threshold value decision circuit **28** of FIG. **7**, and the operation of a threshold value determiner **105** is the same as that of the threshold value determiner **42** of FIG. **17**. Incidentally, the long code candidates in the long code replica generator **101** are limited to those belonging to the long code group obtained by the long code group detector described above.

FIGS. **27**A and **27**B show a synchronization detector of the spreading code synchronization method according to claim **21** of the present invention. It differs from the spreading code synchronization method of FIG. **7** in the following. First, a long code timing detector **106** observes correlation peaks at every L/n chip periods so that the received timing is detected of symbols spread by a shared short code at every interval of L/n chip periods. This enables the capacity of the memory **82** to be reduced.

Second, a long code identification circuit **100**, in which n long code replica generators **101** are supplied with initial set values of the long code phase through (n−1) delay circuits **107**, detects in parallel the correlations between the received signal and the codes obtained by multiplying the long code replicas whose phases are shifted by an amount of L/n from one another by the short code fed from a shared short code replica generator **91**. Then, a maximum correlation value selector **108** selects the maximum correlation value, and a threshold value decision circuit **104** makes a threshold value decision of the maximum correlation value.

As described above, according to the present invention, in the long code system in which the base stations are asynchronous, the mobile station can achieve high speed, high accuracy spreading code synchronization of a forward control channel. Furthermore, since the matched filter is used only for the initial short code search, and a sliding correlator is used for the long code search thereafter, the consumed power by the entire spreading code synchronization detector does not increase so much.

What is claimed is:

1. A signal transmission method in a mobile communication system in a direct sequence CDMA communication system which transmits a wideband signal spread using a spreading code with a rate higher than an information rate, said signal transmission method comprising the steps of: